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/Mark D. Saralino/ **August 11, 2006**
Mark D. Saralino Date

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Graham Andrew CAIRNS et al.

Serial No.: 09/943,535

Filing Date: August 30, 2001

For: DRIVING ARRANGEMENTS FOR ACTIVE MATRIX LCDs

Examiner: Lun Yi Lao

Art Unit: 2673

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Commissioner for Patents
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APPELLANTS' REPLY BRIEF UNDER 37 CFR §41.41

Sir:

Appellants submit this reply brief in response to the Examiner's Answer mailed on June 15, 2006.

I. THE EXAMINER'S ANSWER DOES NOT SUBSTANTIVELY ADDRESS APPLICANTS' ARGUMENTS ON THE MERITS

Appellants note the Examiner's Answer suffers from the same fundamental deficiencies found during prosecution. Basically, the Examiner has and continues to contend that *Nishioka et al.* anticipates or obviates the claims, but seemingly does not substantively address applicants detailed analysis as to why the Examiner's contentions are incorrect. Appellants in their previous responses to Office Actions and in Appellants' Appeal Brief give a very specific and detailed analysis of the device operation in *Nishioka et al.* Moreover, Appellants clearly explain why then the operation in *Nishioka et al.* does not anticipate or render obvious the claimed subject matter.

The Examiner, on the other hand, continues not to address Appellants' detailed analysis in support of Appellants' arguments. The Examiner continues to make the same conclusory arguments and blanket statements regarding the teachings of *Nishioka et al.* The Examiner even disregards how Appellants AGREE with the Examiner in some respects.

The operation of *Nishioka et al.* is fundamental to the issues at hand in this appeal. Appellants have clearly described how *Nishioka et al.* operates in relevant part in Appellants' Appeal Brief. The Examiner has not provided any counter-explanation whatsoever as to how Appellants' description is incorrect. The Examiner simply restates that *Nishioka et al.* operates as recited in the rejected claims, ignoring Appellants' detailed explanation as to why the Examiner's understanding of the operation of *Nishioka et al.* is incorrect.

Appellants note that there cannot be any meaningful furtherance of prosecution if the Examiner does not address the detailed points raised by Appellants during prosecution and appeal. Appellants respectfully submit that Appellants' Brief clearly set forth the distinctions between the present invention and *Nishioka et al.* Appellants clearly set forth how *Nishioka et al.* does NOT operate in the manner maintained by the Examiner.

II. APPELLANTS ADDRESS "NEW" POINTS RAISED IN EXAMINER IN ANSWER

While Appellants submit the Examiner has not substantively addressed Appellants' arguments for the reasons stated above, Appellants offer the following further comments on the points raised in the Examiner's Answer:

***a. Appellants state that Nishioka et al. teaches controlling the particular display mode based on the determination of a user selection on page 10 [of Appellants' Appeal Brief]. However, the claim limitations do not [require] the input data should be automatically generated from a computer. Therefore, [Nishioka et al.] meet all the limitations cited in claims 1, 2, 5, 9, 10 and 12-14. (Examiner's Answer, p. 8)* (Emphasis Added).**

Applicants AGREE that the claims do not recite that "the input data should be automatically generated from a computer". However, claim 1 does recite *"data analysis means arranged to receive said digital input data, to determine the color format of the input data, and to control the data driver to operate in the display mode corresponding to the determined color format of the input data..."*. (Claim 1; emphasis added).

Accordingly, the data analysis means, in addition to (1) receiving digital input data in a plurality of different color formats, also (2) determines the color format of the input data, and (3) controls the data driver to operate in a display mode corresponding to said determined color format. Thus, the data analysis means determines the color format of the input data. The color format determination does not require user selection or input as is done in *Nishioka et al.* (See, e.g., pages 7 and 10 of Appellants' Appeal Brief).

The Examiner's statement that "the claim limitations do not [require] the input data should be automatically generated from a computer", to the extent understood by the Appellants, overlooks the fact that claim 1 *does* require a data analysis means that determines the color format of the input data. There simply is no data analysis means

in *Nishioka et al.* that determines the color format of the input data. Nor is there any data analysis means that then controls the data driver to operate in the display mode corresponding to the determined color format of the input data as recited in claim 1. As Appellants have previously argued in Appellants' Appeal Brief, *Nishioka et al.* teaches operating in a display mode in accordance with a user input selection. The user input selection in *Nishioka et al.* does not constitute an analysis of the input data to determine the color format of the input data.

b. Appellants argue that Nishioka et al. do not teach input data in a plurality of different color format on page 7. The Examiner disagrees in that Nishioka et al. teaches input data (40-43, 24) in a plurality of different color formats (when the input data (40-43, 24) is "H" state, it is indicated 512 color format; when the input data (24) is "L" state, it indicated 4096 color format) (see Figures 1, 5-7; Abstract; Column 8, lines 53-68; Column 9, lines 1-30; Column 11, lines 60-68; Column 12, lines 1-14 and lines 54-68; and Column 13, lines 1-2). (Examiner's Answer, page 6) (Emphasis Added).

The Examiner appears to have missed the Appellants' point entirely. Appellants do NOT argue that *Nishioka et al.* does not teach input data in a plurality of different color format. In fact, Appellants have AGREED with the Examiner. As Appellants state in their brief:

> *Appellants believe it may be helpful to note that they are in complete agreement with the Examiner that Nishioka et al. teaches a display having selectable display modes. Appellants agree that Nishioka et al. teaches the control of different display modes involving different frequencies, input data with different numbers of bits, numbers of colors, etc. However, a fundamental difference between the present invention and Nishioka et al. is how the different display modes are controlled. The driving arrangement of claim 1 utilizes a data analysis means that receives the input data to be displayed and determines the color format of the input data (e.g., whether 1-bit per color; m bits per color; n+m bits per color; etc.). The data analysis means then controls the data driver according to the display mode corresponding to the determined color format. (See, e.g., Fig. 6).*

> *The Examiner continues, in applicants' opinion, to focus incorrectly on the fact that Nishioka et al. provides a display that operates in different display modes rather than focusing on how Nishioka et al. controls the display so as to operate in different display modes. As applicants have argued previously, Nishioka et al. does not control the display mode based on a determination of the color format of the display input data as recited in claim 1. (Appeal Brief, page 7) (Emphasis Added).*

The Examiner's repeated laundry list of citations to *Nishioka et al.* including data of different formats does not address Appellants' point. Appellants agree *Nishioka et al.* teaches different formats. However, *Nishioka et al.* does not teach controlling the display format based on a data analysis means analyzing the input data to determine the color format as recited in claim 1. (See detailed analysis in Appellants' Appeal Brief).

c. Appellants argue that Nishioka et al. do not teach data analysis means which determines the color format of the input data and controls the data to operate in different mods based on the color format of the input data on page 7. The Examiner disagrees with that since Nishioka et al. teach data analysis means (44, see figures 7-8) which determines the color format (512 or 4096) of the input data and controls the data to operate in different modes (512 low color resolution mode or 4096 high color resolution mode) based on the determined color format of the input data (40-43, 24) (see figures 1, 7-8; abstract; column 8, lines 53-58, column 15, lines 10-39 and rejection paragraph 1). (Examiner's Answer, page 6).

Appellants note that the Examiner's response is merely a conclusory recitation of the same citations to *Nishioka et al.* that Appellants already addressed in their explanation of how *Nishioka et al.* operates. As explained in detail in Appellants Appeal Brief, Appellants note:

> *Appellants agree that line 25 in Nishioka et al. admittedly includes the display data which is input to the FRC circuit 44 as illustrated in Fig. 6. However, the FRC circuit 44 functions to provide either 4096 or 512 mode data at its output*

45 based on the signal input on line 24. (See, e.g., Fig. 6 and Col. 8, lns. 55-58 "This circuit 22 delivers the selection information to the display unit 23 through the signal line 24, and designates the number of colors to-be-developed i.e. 4096 or 512").

More specifically, when the signal input on line 24 is in an "H" state, the FRC frame rate control circuit 44 is instructed that the number of colors to be developed is 512. When the signal input on line 24 is in an "L" state, this indicates to the FRC 44 that the number of colors to be developed is 4096. (column 12, lines 3-11; see Fig. 7.). Whether the signal on line 24 is in an "H" or "L" state depends on whether the CPU 1 writes a "1" or "0" to a latch 34 as illustrated in Fig. 5. In other words, the CPU 1 writes a "1" to the latch 34 when the number of colors to be developed is 512, and writes a "0" to the latch circuit 34 when the number of colors to be developed is 4096. (see, e.g., column 12, lines 11-14, "the number 512 of the colors can be set when the CPU 1 writes "1" into the allocated address of the latch circuit 34, while the number 4096 can be set when it writes "0"").

Thus, Appellants respectfully submit that whether the FRC circuit 44 produces 4096 colors or 512 colors depends on whether the CPU 1 writes a "1" or "0" to the FRC circuit 44. Clearly, therefore, the FRC circuit 44 is not acting as a "data analysis means" of claim 1 as argued by the Examiner. The FRC circuit 44 is operating in 4096/80Hz mode or 512/60Hz mode based on the input on line 24. The FRC circuit 44 is not receiving the display input data and determining the color format of the input data as recited in claim 1. (Appellants' Appeal Brief, pages 9-10).

The Examiner does not address how or why the Appellants' explanation of the teachings of *Nishioka et al.* is incorrect. Rather, the Examiner simply replies with the same laundry list of citations to the reference. The Examiner does not respond to the fact that the very citations to which the Examiner refers teach the distinctions argued by the Appellants. Again, absent any meaningful rebuttal to Appellants' arguments, it is difficult to engage in any meaningful resolution to the issues at hand.

d. Appellants argue that Nishioka et al. does not teach a driving arrangement controls the data driver to consume less power in low resolution display mode and more power in high resolution display mode based on the determined color format of the input data on

page 7. The examiner disagrees with that since Nishioka et al. teach a driving arrangement controls the data driver to consume less power in low resolution display mode (512 color mode) and more power in high resolution display mode (4096 color mode) based on the determined color format of the input data (40-43, 24) (see figures 1, 4, 6-8; abstract and column 10, lines 5-47). (Examiner's Answer, page 7).

As is hopefully clear by now, Appellants did NOT argue that *Nishioka et al.* does not teach a low resolution display mode and a high resolution display mode. Appellants agree that *Nishioka et al.* teaches a low resolution display mode and a high resolution display mode.

Rather, Appellants are arguing that *Nishioka et al.* does not control low and high resolution operation based on a data analysis means that determines the color format of the input data as recited in claim 1. In maintaining the rejection, the Examiner simply refers to the same citations in *Nishioka et al.* The Examiner does not address applicants detailed analysis as to why such citations do not represent a data analysis means for determining the color format of the input data as recited in claim 1. The Boards' attention is directed to pages 8-10 of Appellants' Appeal Brief which explains in detail the relevant differences between *Nishioka et al.* and the claimed invention. As is explained, *Nishioka et al.* controls the display mode based on factors independent of the color format of the input data itself.

e. Appellants state that the FRC circuit (44) produces 4096 or 512 colors depends on whether the CPU 1 write a "1" or "0" to the FRC circuit 44 on page 10. The examiner disagrees with that since Nishioka et al. teach the FRC circuit (44) produces 4096 or 512 colors depends on the input data (24) whether it is "0" or "1" (see figures 1, 5-8; column 12, lines 8-14 and column 15, lines 10-39). (Examiner's Answer, page 8).

The above portion of the Examiner's Answer appears to be the only section that touches upon the details of Appellants' arguments. Although reluctant to oversimplify

the issues at hand, appellants note that a fundamental distinction between the present invention and *Nishioka et al.* relates to how or why the data on line 24 in *Nishioka et al.* becomes a "0" or "1". Appellants describe in detail the operation of *Nishioka et al.* in their Appeal Brief. Specifically, Appellants point out how and when the signal on line 24 is a "0" or a "1". To wit, appellants point out:

> *The Board may be interested to know how or under what circumstances does the CPU 1 in Nishioka et al. write a "1" or a "0" to the FRC circuit 44. As Appellants have pointed out in their previous responses, whether the CPU 1 writes a "1" or "0" to the FRC circuit 44 is based on user selection, power source selection, whether the device is in an idle or sleep mode, etc. More specifically, Nishioka et al. teaches controlling the particular display mode based on the determination of a user selection (column 9, lines 52-59); a power source (column 10, lines 5-21); and an idle or sleep mode (column 11, lines 40-44). Such means for selection are further emphasized in the claims of Nishioka et al. where the claims recite mode selection based on user selection, power source, idle or sleep mode, etc. (See, e.g., claims 3-5, 20 and 22).*
>
> *Nishioka et al. simply does not teach or suggest that the CPU 1, the FRC circuit 44, or anything else controls the display mode based on analyzing the display input data itself so as to determine the color format of the input data as recited in claim 1. (Appellants' Appeal Brief, page 10).*

Contrary to the position taken by the Examiner, the data on line 24 is not "input data" in the context of the present invention. The input data of claim 1 is the input data that can have a plurality of different color formats and provides a display image. The data on line 24 in *Nishioka et al.* is not input data. Rather, the data on line 24 is a control bit issued by the CPU 1. Whether the CPU 1 issues a control bit of "0" or "1" on line 24 is not based on an analysis of the input data to determine a color format of the input data. (See explanation above and in Appellants' Appeal Brief).

Accordingly, Appellants again emphasize that *Nishioka et al.* does not provide control of the different display modes based on a data analysis means that determines the color format of the display input data. *Nishioka et al.* teaches controlling the particular display mode based on the determination of a user selection (column 9, lines 52-59); a power source (column 10, lines 5-21); and an idle or sleep mode (column 11,

lines 40-44). Such means for selection are further emphasized in the claims of *Nishioka et al.* where the claims recite mode selection based on user selection, power source, idle or sleep mode, etc. (See, e.g., claims 3-5, 20 and 22).

Nishioka et al. simply does not teach or suggest that the CPU 1, the FRC circuit 44, or anything else controls the display mode based on analyzing the display input data itself so as to determine the color format of the input data as recited in claim 1.

Appellants therefore again respectfully request reversal and withdrawal of the rejection of claim 1. The remaining claims each depend from claim 1 either directly or indirectly, and therefore are allowable for at least the same reasons. The secondary references do not make up for the deficiencies in *Nishioka et al.*

Should a petition for an extension of time be necessary (or if such a petition has been made and an additional extension is necessary), petition is hereby made and the Commissioner is authorized to charge any fees (including additional claim fees) to Deposit Account No. 18-0988.

Respectfully submitted,

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DATE: August 11, 2006

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